CBCS Scheme

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15CS32

Third Semester B.E. Degree Examination, June/July 2017
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Explain with help of a circuit diagram and characteristic curves working of N-channel DE MOSFET. **(12 Marks)**

b. List and explain any one application of FET and its working with circuit Diagram. **(04 Marks)**

OR

2 a. Explain the performance parameters of operational amplifier. **(08 Marks)**

b. Mention and explain the working of any two applications of operational amplifier. **(08 Marks)**

Module-2

3 a. What is a logical gate? Realize $((A+B)\cdot C)D$ using only NAND Gates. **(04 Marks)**

b. Describe positive and Negative logic. List the equivalences between them. **(04 Marks)**

c. Find the minimal SOP (sum of product) for the following Boolean functions using K-map

i) $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11)$

ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 10) + d(0, 15)$ **(08 Marks)**

OR

4 a. Using Quine – MCClusky Method simplify the following Boolean equation.
$f(a, b, c, d) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$. **(10 Marks)**

b. Define Hazard. Explain Different Types of Hazards. **(06 Marks)**

Module-3

5 a. What is multiplexer? Design a 32 to 1 multiplexer (MUX) using two 16 to 1 MUX and one 2 to 1 MUX. **(04 Marks)**

b. Show How using 3 to 8 Decoder and multi input OR gates, following Boolean Expressions can be realized simultaneously
$F_1(a, b, c) = \sum m(0, 4, 6)$, $F_2(a, b, c) = \sum m(0, 5)$, $F_3(a, b, c) = \sum m(1, 2, 3, 7)$ **(05 Marks)**

c. Design 7 segment Decoder using PLA. **(07 Marks)**

OR

6 a. Implement the Boolean function expressed by SOP $f(a, b, c, d) = \sum m(1, 2, 5, 6, 9, 12)$ using 8 : 1 MUX. **(04 Marks)**

b. What is magnitude comparator? Design and explain 2 bit magnitude comparator. **(08 Marks)**

c. Differentiate between combinational and sequential circuit. **(04 Marks)**

Module-4

7 a. With a neat logic diagrams and truth table. Explain the working of JK master slave Flip-Flop along with its implementation using NAND Gates. **(10 Marks)**

b. Derive the characteristic equation for SR, D and JK Flip-Flop. **(06 Marks)**

OR

8 a. Using Negative Edge triggered D-Flip Flop. Draw a Logic diagram of 4 bit serial in serial out (SISO) Register. Draw the waveform to shift Binary number 1010 into this register. **(06 Marks)**

b. Explain with neat diagram How shift Register can be applied for serial addition. **(07 Marks)**

c. Differentiate between synchronous and Asynchronous counter. **(03 Marks)**

Module-5

9 a. Design Asynchronous counter for the sequences $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$. Using S. R Flip-Flop. **(12 Marks)**

b. With neat diagram. Explain Digital Clock. **(04 Marks)**

OR

10 a. Explain 2 bit simultaneous A/D converter. **(10 Marks)**

b. What is Binary Ladder? Explain the Binary Ladder with Digital input of 1000. **(06 Marks)**

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